WHAT IS CLAIMED IS:

1. A method of generating a codeword for transmission in a communications system, the method comprising:

generating a first set of error detection check bits from one or more information bits;

generating a second set of error detection check bits from the one or more information bits and the first set of error detection check bits; and

concatenating the one or more information bits, the first set of error detection check bits and the second set of error detection check bits.

2. The method of claim 1 further comprising:

generating a third set of error detection check bits from the one or more information bits, the first set of error detection check bits and the second set of error detection check bits; and

concatenating the third set of error detection check bits with the concatenated one or more information bits, first set of error detection check bits, and second set of error detection check bits.

3. The method of claim 1, further comprising:

generating a header that includes an indication of how many sets of error detection check bits there are in the codeword; and

concatenating the header with the concatenated one or more information bits, first set of error detection check bits, and second set of error detection check bits.

4. The method of claim 1, further comprising:

generating an indication of how many sets of error detection check bits there are in the codeword;

associating the generated indication with the concatenated one or more information bits, first set of error detection check bits, and second set of error detection check bits.

5. The method of claim 1, further comprising:

by means of an error correction code, encoding the one or more information bits, the first set of error detection check bits and the second set of error detection check bits.

6. The method of claim 1, wherein at least one of the first set of error detection check bits and the second set of error detection check bits is generated by means of a cyclic redundancy check code.

7. A method of receiving a codeword that comprises one or more information bits, a first set of error detection check bits and a second set of error detection check bits, the method comprising:

using the first set of error detection check bits to make a first determination whether the one or more information bits are error-free;

using the second set of error detection check bits to make a second determination whether the one or more information bits and the first set of error detection check bits are error-free; and

accepting the one or more information bits only if the first determination indicates that the one or more information bits are error-free and the second determination indicates that the one or more information bits and the first set of error detection check bits are error-free.

8. The method of claim 7, further comprising:

determining whether a first level of error detection or a second level of error detection is to be used, and

wherein using the second set of error detection check bits to make the second determination whether the one or more information bits and the first set of error detection check bits are error-free, and accepting the one or more information bits only if the first determination indicates that the one or more information bits are error-free and the second determination indicates that the one or more information bits and the first set of error detection check bits are error-free are performed only if the second level of error detection is to be used.

9. The method of claim 8, further comprising:

if the first level of error detection is to be used, then accepting the one or more information bits if the first determination indicates that the one or more information bits are error-free.

10. The method of claim 8, wherein determining whether the first level of error detection or the second level of error detection is to be used comprises:

determining whether the codeword is a retransmitted codeword.

11. The method of claim 8, wherein determining whether the first level of error detection or the second level of error detection is to be used comprises:

determining how many times the codeword was retransmitted.

12. The method of claim 8, wherein:

the codeword includes an indication of how many sets of error detection check bits there are in the codeword; and

determining whether the first level of error detection or the second level of error detection is to be used comprises using the indication in the codeword to determine whether the first level of error detection or the second level of error detection is to be used.

13. The method of claim 8, wherein:

the codeword was received in a packet;

the packet further includes a header;

the header includes an indication of how many sets of error detection check bits there are in the codeword; and

determining whether the first level of error detection or the second level of error detection is to be used comprises using the indication in the header to determine whether the first level of error detection or the second level of error detection is to be used.

14. The method of claim 7, wherein:

the codeword was generated by means of an error correction code that was applied to the one or more information bits, the first set of error detection check bits and the second set of error detection check bits;

and the method further comprises:

decoding the codeword using the error correction code.

15. The method of claim 7, wherein at least one of the first set of error detection check bits and the second set of error detection check bits is a set of cyclic redundancy check bits.

16. A method of receiving a codeword that comprises one or more information bits and a plurality of sets of error detection check bits, wherein each of the sets of error detection check bits is associated with a corresponding portion of the codeword, the method comprising:

determining how many error detection checks should be performed;

until the determined number of error detection checks are performed, repeatedly using a different one of the sets of error detection check bits to

determine whether the corresponding portion of the received codeword contains an error; and

disregarding all remaining unused different ones of the sets of error detection check bits.

17. The method of claim 16, wherein determining how many error detection checks should be performed comprises determining whether the received codeword is a retransmitted codeword.

18. The method of claim 16, wherein determining how many error detection checks should be performed comprises determining how many times the received codeword has been retransmitted.

19. The method of claim 16, wherein:

the codeword includes an indication of how many sets of error detection check bits there are in the codeword; and

determining how many error detection checks should be performed comprises using the indication in the codeword to determine how many error detection checks should be performed.

20. The method of claim 16, wherein:

the codeword was received in a packet;

the packet further includes a header;

the header includes an indication of how many sets of error detection check bits there are in the codeword; and

determining how many error detection checks should be performed comprises using the indication in the header to determine how many error detection checks should be performed.

21. An apparatus for generating a codeword for transmission in a communications system, the apparatus comprising:

a first error detection code generator that generates a first set of error detection check bits from one or more information bits;

a second error detection code generator that generates a second set of error detection check bits from the one or more information bits and the first set of error detection check bits; and

logic that concatenates the one or more information bits, the first set of error detection check bits and the second set of error detection check bits.

22. The apparatus of claim 21, further comprising:

a third error detection code generator that generates a third set of error detection check bits from the one or more information bits, the first set of error detection check bits and the second set of error detection check bits; and

logic that concatenates the third set of error detection check bits with the concatenated one or more information bits, first set of error detection check bits, and second set of error detection check bits.

23. The apparatus of claim 21, further comprising:

a header generator that generates a header that includes an indication of how many sets of error detection check bits there are in the codeword; and

logic that concatenates the header with the concatenated one or more information bits, first set of error detection check bits, and second set of error detection check bits.

24. The apparatus of claim 21, further comprising:

an indication generator that generates an indication of how many sets of error detection check bits there are in the codeword;

logic that associates the generated indication with the concatenated one or more information bits, first set of error detection check bits, and second set of error detection check bits.

25. The apparatus of claim 21, further comprising:

an error correction code generator that encodes the one or more information bits, the first set of error detection check bits and the second set of error detection check bits.

26. The apparatus of claim 21, wherein at least one of the first error detection code generator and the second error detection code generator is a cyclic redundancy check code generator.

27. An apparatus for receiving a codeword that comprises one or more information bits, a first set of error detection check bits and a second set of error detection check bits, the apparatus comprising:

logic that uses the first set of error detection check bits to make a first determination whether the one or more information bits are error-free;

logic that uses the second set of error detection check bits to make a second determination whether the one or more information bits and the first set of error detection check bits are error-free; and

logic that accepts the one or more information bits only if the first determination indicates that the one or more information bits are error-free and the second determination indicates that the one or more information bits and the first set of error detection check bits are error-free.

28. The apparatus of claim 27, further comprising:

logic that determines whether a first level of error detection or a second level of error detection is to be used, and

wherein the logic that uses the second set of error detection check bits to make the second determination whether the one or more information bits and the first set of error detection check bits are error-free, and the logic that accepts the one or more information bits only if the first determination indicates that the one or more information bits are error-free and the second determination indicates that the one or more information bits and the first set of error detection check bits are error-free operate only if the second level of error detection is to be used.

29. The apparatus of claim 28, further comprising:

logic that responds to a determination that the first level of error detection is to be used by accepting the one or more information bits if the first determination indicates that the one or more information bits are error-free.

30. The apparatus of claim 28, wherein the logic that determines whether the first level of error detection or the second level of error detection is to be used comprises:

logic that determines whether the codeword is a retransmitted codeword.

31. The method of claim 28, wherein the logic that determines whether the first level of error detection or the second level of error detection is to be used comprises:

logic that determines how many times the codeword was retransmitted.

32. The apparatus of claim 28, wherein:

the codeword includes an indication of how many sets of error detection check bits there are in the codeword; and

the logic that determines whether the first level of error detection or the second level of error detection is to be used comprises logic that uses the

indication in the codeword to determine whether the first level of error detection or the second level of error detection is to be used.

33. The apparatus of claim 28, wherein:

the codeword was received in a packet;

the packet further includes a header;

the header includes an indication of how many sets of error detection check bits there are in the codeword; and

the logic that determines whether the first level of error detection or the second level of error detection is to be used comprises logic that uses the indication in the header to determine whether the first level of error detection or the second level of error detection is to be used.

34. The apparatus of claim 27, wherein:

the codeword was generated by means of an error correction code that was applied to the one or more information bits, the first set of error detection check bits and the second set of error detection check bits;

and the apparatus further comprises:

logic that decodes the codeword using the error correction code.

35. The apparatus of claim 27, wherein at least one of the first set of error detection check bits and the second set of error detection check bits is a set of cyclic redundancy check bits.

36. An apparatus for receiving a codeword that comprises one or more information bits and a plurality of sets of error detection check bits, wherein each of the sets of error detection check bits is associated with a corresponding portion of the codeword, the apparatus comprising:

logic that determines how many error detection checks should be performed; and

error detection logic that operates until the determined number of error detection checks are performed, by repeatedly using a different one of the sets of error detection check bits to determine whether the corresponding portion of the received codeword contains an error,

wherein the error detection logic disregards all remaining unused different ones of the sets of error detection check bits.

37. The apparatus of claim 36, wherein the logic that determines how many error detection checks should be performed comprises logic that determines whether the received codeword is a retransmitted codeword.

38. The apparatus of claim 36, wherein the logic that determines how many error detection checks should be performed comprises logic that determines how many times the received codeword has been retransmitted.

39. The apparatus of claim 36, wherein:

the codeword includes an indication of how many sets of error detection check bits there are in the codeword; and

the logic that determines how many error detection checks should be performed comprises logic that uses the indication in the codeword to determine how many error detection checks should be performed.

40. The apparatus of claim 36, wherein:

the codeword was received in a packet;

the packet further includes a header;

the header includes an indication of how many sets of error detection check bits there are in the codeword; and

the logic that determines how many error detection checks should be performed comprises logic that uses the indication in the header to determine how many error detection checks should be performed.